In the Claims:

Claims 1-12 (Cancelled).

13. (New) An electronic circuit comprising:

an input logic inverter operating at a first voltage level and having an input and an output, the input for receiving an input signal at the first voltage level;

an output logic inverter operating at a second voltage level lower than the first voltage level and having an input and an output for providing an output signal of the electronic circuit; and

voltage reduction means connected between the output of said input logic inverter and the input of said output logic inverter;

said input logic inverter, said output logic inverter, and said voltage reduction means cooperating to reduce the input signal from the first voltage level to the second voltage level to provide the output signal so that the input and output signals have substantially equal rise and fall delays and substantially equal rise and fall transition times.

14. (New) The electronic circuit of Claim 13 wherein said voltage reduction means comprises a plurality of series-connected transistors each biased to provide a fixed voltage drop.

15. (New) The electronic circuit of Claim 14 wherein said voltage reduction means further comprises a

feedback transistor connected between the output and input of said output logic inverter to reduce output leakage current therefrom.

16. (New) The electronic circuit of Claim 13 wherein said voltage reduction means reduces a voltage level of the input signal to between a first threshold below the first voltage level and a second threshold above the first voltage level.

17. (New) The electronic circuit of Claim 16 wherein said output logic inverter comprises at least one output transistor, and wherein the second threshold corresponds to an upper voltage limit for said at least one output transistor.

18. (New) The electronic circuit of Claim 16 wherein said output logic inverter comprises at least one output transistor, and wherein the first threshold corresponds to a threshold voltage of said at least one output transistor.

19. (New) The electronic circuit of Claim 13 further comprising:

a first logic circuit operating at the first voltage level and providing the input signal to the input of said input logic inverter; and

a second logic circuit operating at the second voltage level for receiving the output signal from the output of said output logic inverter.

20. (New) The electronic circuit of Claim 13 wherein said voltage reduction means provides an output signal that follows an output signal of said input logic inverter until reaching the second voltage level and remains at the second voltage level while the output signal of said input logic inverter remains above the second voltage level.

21. (New) The electronic circuit of Claim 20 wherein said voltage reduction means comprises:

a first transistor having a first conduction terminal connected to the second voltage level, a second conduction terminal connected to the input of said output logic inverter, and a control terminal connected to the output of said input logic inverter; and

a second transistor having a first conduction terminal for receiving the input signal, a second conduction terminal connected to the input of said output logic inverter, and a control terminal connected to the output of said input logic inverter.

22. (New) An electronic circuit comprising:

an input inverter operating at a first voltage level and having an input and an output, the input for receiving an input signal at the first voltage level;

an output inverter operating at a second voltage level lower than the first voltage level and having an input and an output for providing an output signal of the electronic circuit; and

a voltage reduction circuit connected between the output of said input inverter and the input of said output inverter;

said input inverter, said output inverter, and said voltage reduction circuit cooperating to reduce the input signal from the first voltage level to the second voltage level to provide the output signal so that the input and output signals have at least one of substantially equal rise and fall delays and substantially equal rise and fall transition times.

23. (New) The electronic circuit of Claim 22 wherein said voltage reduction circuit comprises a plurality of series-connected transistors each biased to provide a fixed voltage drop.

24. (New) The electronic circuit of Claim 23 wherein said voltage reduction circuit further comprises a feedback transistor connected between the output and input of said output logic inverter.

25. (New) The electronic circuit of Claim 22 wherein said voltage reduction circuit reduces a voltage level of the input signal to between a first threshold below the first voltage level and a second threshold above the first voltage level.

26. (New) The electronic circuit of Claim 25 wherein said output inverter comprises at least one output

transistor, and wherein the second threshold corresponds to an upper voltage limit for said at least one output transistor.

27. (New) The electronic circuit of Claim 25 wherein said output inverter comprises at least one output transistor, and wherein the first threshold corresponds to a threshold voltage of said at least one output transistor.

28. (New) The electronic circuit of Claim 22 further comprising:

a first logic circuit operating at the first voltage level and providing the input signal to the input of said input inverter; and

a second logic circuit operating at the second voltage level for receiving the output signal from the output of said output inverter.

29. (New) The electronic circuit of Claim 22 wherein said voltage reduction circuit provides an output signal that follows an output signal of said input inverter until reaching the second voltage level and remains at the second voltage level while the output signal of said input inverter remains above the second voltage level.

30. (New) The electronic circuit of Claim 29 wherein said voltage reduction circuit comprises:

a first transistor having a first conduction terminal connected to the second voltage level, a second conduction terminal connected to the input of said output

inverter, and a control terminal connected to the output of said input inverter; and

a second transistor having a first conduction terminal for receiving the input signal, a second conduction terminal connected to the input of said output inverter, and a control terminal connected to the output of said input inverter.

31. (New) A voltage conversion method comprising:

providing an input inverter and an output inverter each having a respective input and output, the input inverter operating at a first voltage level and the output inverter operating at a second voltage level lower than the first voltage level;

connecting a voltage reduction circuit between the output of the input inverter and the input of the output inverter; and

connecting an input signal at the first voltage level to the input of the input inverter so that the input inverter, the output inverter, and the voltage reduction circuit cooperate to reduce the input signal from the first voltage level to the second voltage level to provide the output signal with the input and output signals having at least one of substantially equal rise and fall delays and substantially equal rise and fall transition times.

32. (New) The method of Claim 31 wherein the voltage reduction circuit comprises a plurality of series-

connected transistors each biased to provide a fixed voltage drop.

33. (New) The method of Claim 32 wherein the voltage reduction circuit further comprises a feedback transistor connected between the output and input of the output inverter.

34. (New) The method of Claim 33 wherein the voltage reduction circuit reduces a voltage level of the input signal to between a first threshold below the first voltage level and a second threshold above the first voltage level.

35. (New) The method of Claim 33 wherein the output logic inverter comprises at least one output transistor, and wherein the second threshold corresponds to an upper voltage limit for the at least one output transistor.

36. (New) The method of Claim 31 wherein the voltage reduction circuit provides an output signal that follows an output signal of the input inverter until reaching the second voltage level and remains at the second voltage level while the output signal of the input inverter remains above the second voltage level.

37. (New) The method of Claim 36 wherein the voltage reduction circuit comprises:

a first transistor having a first conduction terminal connected to the second voltage level, a second

conduction terminal connected to the input of the output inverter, and a control terminal connected to the output of the input inverter; and

a second transistor having a first conduction terminal for receiving the input signal, a second conduction terminal connected to the input of the output inverter, and a control terminal connected to the output of the input inverter.